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CONCEPTION AND REALIZATION EIGHT STAGE DC-AC INVERTER USING OFSVPWM

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ABSTRACT:

This image depicts a DC-AC converter that uses a multi-stage SVPWM topology. The suggested multilayer inverter has the potential to produce seven distinct AC output voltages, depending on the gate signals used. A low pass filter might possibly lessen the amount of harmonic distortion in the output voltage by working with a sinusoidal input voltage. By lowering voltage stress on power components, the suggested multi-level inverter might cut down on energy wasted as switching losses. The suggested inverter's operating principles and method for balancing the voltage across the input capacitors are laid forth. The prototype multilayer inverter accepts 400 V of input voltage and produces 220 V rms at 2 kW of power. Space Vector Pulse-Width Modulation (SVPWM) is a possible method for adjusting the pulse width of the multilayer inverter. Maximum efficiency is predicted to be 98.9%, while full load efficiency is expected to be 97.6%.

Keywords:

The DC-to-AC converter employs Space Vector Pulse Width Modulation (SVPWM) and Maximum Power Point Tracking (MPPT).

I. Introduction

Consistently high-quality electrical power has been more widely available as a result of rapid technological improvement. The rapid development of the semiconductor industry has led to significant improvements in the requirements for power devices and the techniques used to convert power. A specific kind of power converter, inverters change DC electricity into AC current. Figure 1 shows how a RE is linked to conventional loads (uninterruptible power supply [UPS], servomotor(s), air conditioner(s), and smart grid). Depending on the characteristics and needs of the load, the frequency and voltage at the output must dynamically change. [1]-[3]. Everyone has at least one power tool these days. The already serious problem of harmonic pollution in the U.S. electrical system is made much worse by this. Several rules and standards control harmonics and power factor in electrical equipment. These include IEEE Std. 1547, UL 1741, and others. [4]-[6]. Not only have standards for power tools increased in stringency across several sectors, but so have their applications. Power ratings and voltage stress tolerance are two areas where IGBTs excel, but their limited working frequency range is a drawback. Developing a trustworthy gate driver for an IGBT has its own unique difficulties. Even though MOSFET has a lower power rating than IGBT, it performs better in high-frequency applications. Many multilevel topologies get around this issue by putting low-rated components in high-power uses. A multilayer design for a power switch might allow for a reduction in the required operating voltage. That's why it's only used as a last resort. Blending voltages at different outputs may reduce switching frequency, input current distortion, and dv/dt. Numerous new topologies have emerged in recent years as a result of the benefits of multilevel topology [7], [8]. This study

introduces an innovative strategy for designing and deploying multilayer inverters. The lack of supplementary power sources is a fundamental difference between the suggested topology and others.

II.THE KEY PLAYERS

1. Circuit Layout

Figure 2 shows the updated design for the seven-level inverter. C1, C2, and C3 are three capacitors connected in series that act as an input voltage divider. The voltage is divided by four MOSFET and four diodes before it reaches the H-bridge. The power at the circuit's conclusion comes from an H-bridge made up of four MOSFET. With the right setup for the gate signals, the proposed multilayer inverter may provide seven different AC output voltages.

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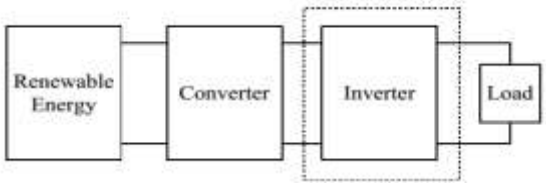


Figure 1: Block schematic of a renewable system

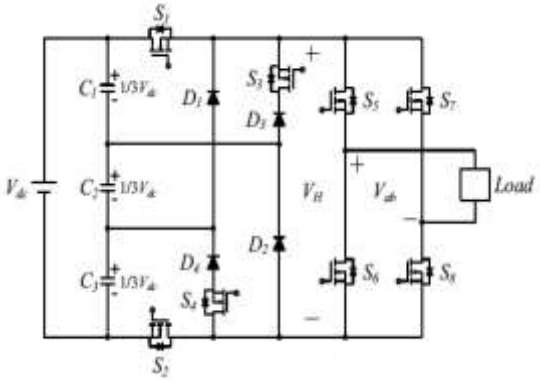
B. Operating Principles

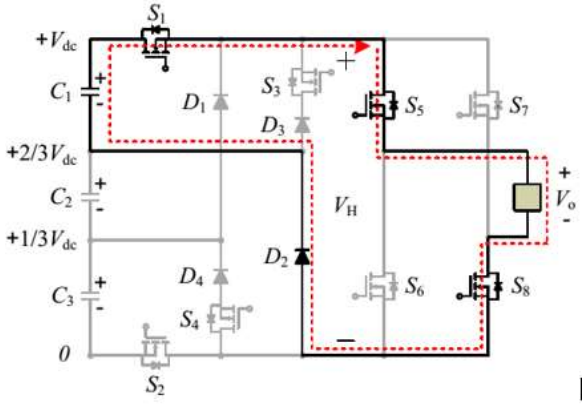
The following is a breakdown of how to produce the seven distinct voltage levels that are needed:

1) By activating S 1 during the positive half cycle, the voltage level V o = 1/3V dc is produced. A regulated 1/3V dc supply is stored in capacitor C1 and used to power the H-bridge. The load terminals get a dc voltage of 0.3 volts when switches S5 and S8 are closed. The route taken in this manner is shown in Fig. 3. When both switches are activated, the resulting voltage is equal to two-thirds of a DC voltage (V o = 2/3V dc). Capacitors C1 and C2 store the power for later use. H-bridges need a dc voltage of 2.7V. Switches S5 and S8 send 2/3V dc to the load terminals when activated. Current transportation is shown in Fig. 4. It is possible to achieve a voltage of V o = V dc if we switch on both S 1 and S 2. C1, C2, and C3 are capacitors that hold the energy. For an H-bridge to operate, the dc voltage across it must be V. With switches 5 and 8 closed, V dc is being sent to the load terminals. Figure 5 depicts a typical example of the current trajectory's pattern. During the negative half cycle, S 2 produces a voltage of V o = -1/3V dc. The H-bridge gets the required 0.3V dc operating voltage from capacitor C3. As illustrated in Fig. 6, with switches 6 and 7 engaged, the load terminals are receiving -1/3V dc.

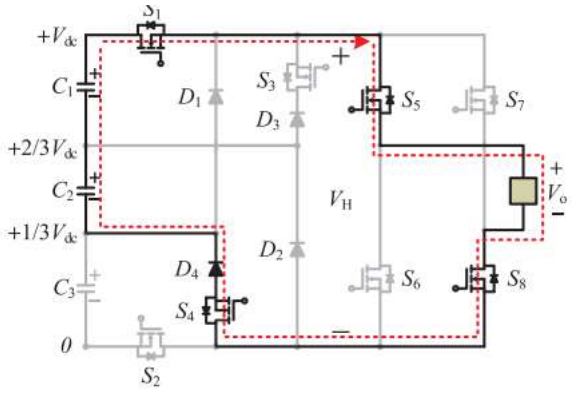
For instance, if both S2 and S3 are active, V o may be -2/3V dc. The power comes from capacitors C2 and C3. H-bridges need a dc voltage of 2.7V. When both switches (S6 and S7) are on, the load terminals get a dc value of -2/3V. The path we are now following may be seen in Figure 7. Six points are awarded when the switches S1 and S2 are used to generate a voltage of V o = -V dc. A dc voltage of V is generated by the three capacitors C1, C2, and C3 and used to power the H-bridge. When switches 6 and 7 are held down, a dc voltage of -V is applied to the load terminals. The path we're on right now is shown in Fig. 8. It's possible that the voltage is zero if switches 5 and 7

are activated. The load terminals are not receiving any power. In Fig. 9, we can see the current's propagation in this manner. The resultant volume levels for each toggle are shown in Table I.





Inverter structure with seven stages is shown in Fig. 2.



The switching setup with an output voltage of 0.3Vdc is shown in Figure 3.

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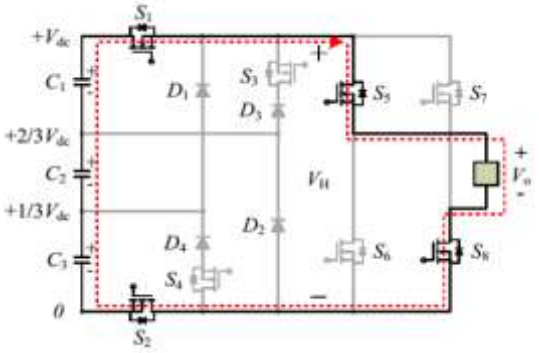

Figure 4: 2/3Vdc Output Voltage Switching Combination

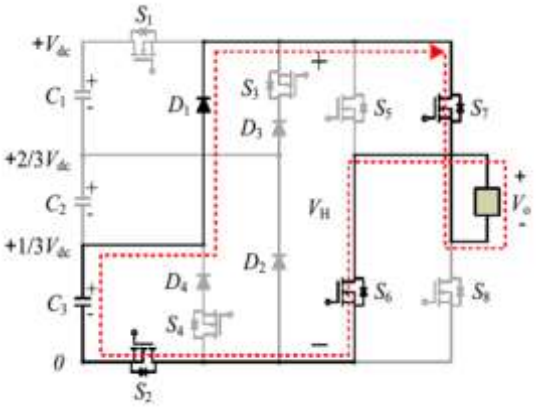

Figure 5 shows a possible output voltage Vdc switching configuration.

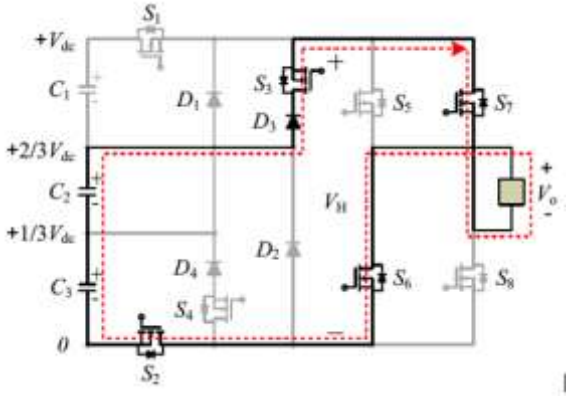

Figure 6: -1/3Vdc Output Voltage Switching Combination

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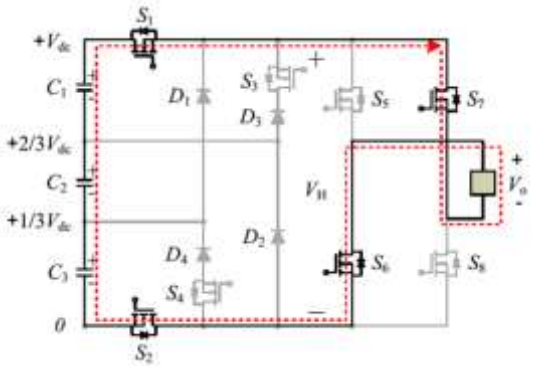


Figure 7: Output switching combination at -2/3Vdc.

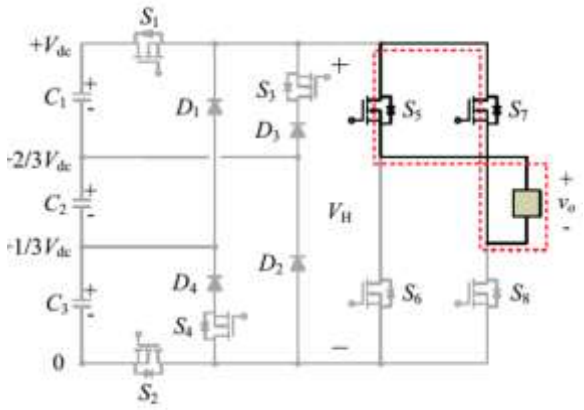


Figure 8: -Vdc Output Voltage Level Switching Combination

The Zero Voltage Output Switching Combo is seen in Figure 9.

TABLE I

The necessary switching configurations for producing a seven-step output voltage waveform

	Switching combinations							
Output voltage V_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$1/3V_{dc}$	on	off	off	off	on	off	off	on
$2/3V_{dc}$	on	off	off	on	on	off	off	on
V_{dc}	on	on	off	off	on	off	off	on
$-1/3V_{dc}$	off	on	off	off	off	on	on	off
$-2/3V_{dc}$	off	on	on	off	off	on	on	off
$-V_{dc}$	on	on	off	off	off	on	on	off
0	off	off	off	off	on	off	on	off

C. Topology Comparison

The suggested topology, as well as the diode-clamped inverter, the capacitor-clamped inverter, and the cascaded multi-cell inverter, are all examples of conventional multilevel topologies [9, 10]. Component counts for these seven-stage inverter systems are shown in Table II. The redesigned layout requires fewer power devices, as seen in Table II. Table III compares the voltage stresses caused by various inverter types.

TABLE II

FOUR VARIOUS SEVEN-LEVEL INVERTERS COMPARED BY THEIR PARTS

	Proposed	Diode-clamped	Capacitor-Clamped	Cascaded multicell
Input sources	1	1	1	3
Input capacitors	3	6	2	3
Clamped capacitors	0	0	5	0
Power switches	8	12	12	12
Diodes	4	10	0	0

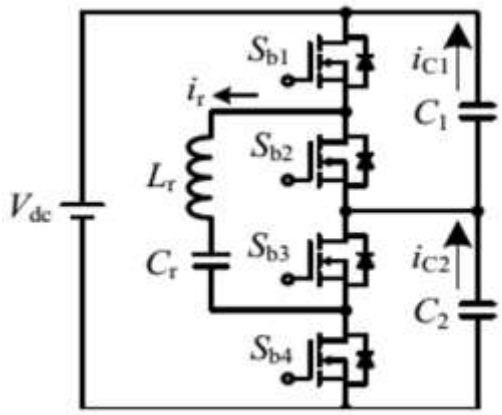
TABLE III

comparison of voltage stress across four distinct seven-level inverters

	Proposed	Diode-clamped	Capacitor-Clamped	Cascaded multicell
Input sources	V_{in}	$2V_{in}$	$2V_{in}$	$V_{in}/3$
Input capacitors	$V_{in}/3$	$V_{in}/3$	$V_{in}/2$	$V_{in}/3$
Power switches	V_{in}	$V_{in}/3$	$V_{in}/3$	$V_{in}/3$
Diodes	$2V_{in}/3$	$3V_{in}/2$	N/A	N/A

III. VOLTAGE BALANCING CIRCUIT

Voltage changes cause harmonics distortion, hence the RSC Sponsored Voltage balancing circuits [11, 15] are necessary for all multilayer inverter capacitors. By use of a resonant switching capacitor converter, the voltage across the input capacitor is equalized. Fig. 10 depicts the RSCC unit's circuits. Each switch is only on for 50% of the time. C1 is preferable than C2 since C2 has a much lower voltage. Most of the charges go from C1 to C2 because the average current in C1 is larger than the current in C2 during a single switching cycle. After a specific number of cycles, the difference in voltage between C1 and C2 will close. Figure 11 depicts RSCC waveforms.



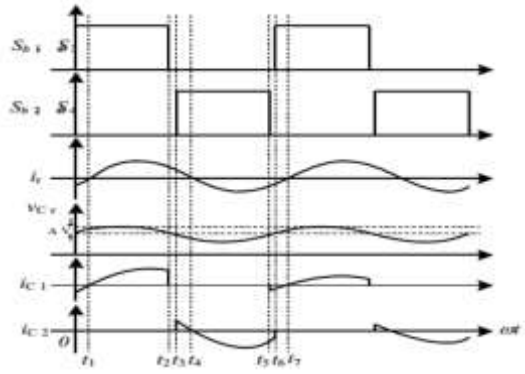


Figure 10 depicts the RSCC circuit design.

Fig. 11 shows the RSCC's circuit configuration.

This schematic depicts the RSCC seven-level inverter. A seven-level RSCC requires a resonant inductor L r, a resonant capacitor Cr, and two more switches S b5 and S b6. Switches S b1, S b3, and S b5 are turned on, along with switches S b2, S b4, and S b6. Toggles need to chip in equitably.

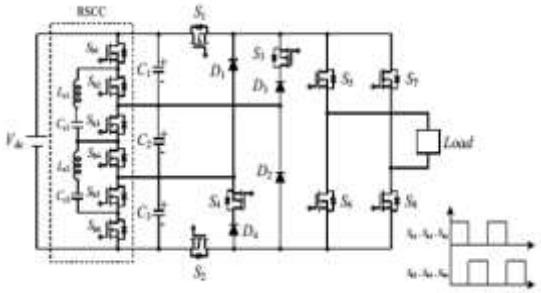


Fig. 12. The proposed multilevel inverter with RSCC.

IV. SVPWM TECHNQUE

The gate pulse waveforms for each PWM cycle are generated by the Space Vector PWM generator module

in response to modulation index instructions. In this part, you'll find detailed information regarding the SVPWM method. A three-phase two-level inverter's output voltage may be in one of eight different switching states. The inverter's full voltage states, V1–V6, are represented by V1–V6 on the plane of all possible Space Vectors, whereas V7–V8 represent the inverter's no voltage states. Each of the six operational vectors (V1-V6) has a dc bus voltage (Vdc) of 23 Vdc. The SVPWM subsystem cannot function without the U Alpha and U Beta signals. The picture displays the gain of the SVPWM module. Both the voltage ratio (V/Vdc) and the modulation index (normalized from V/Vdc) are shown vertically along the M axis. The following formula may be used as an approximate estimate of the line-to-line RMS output voltage (Vline):

$$V_{line} = U_{mag} * Mod_{Scl} * v_{dc}/\sqrt{6}/2^{25} \quad (22)$$

when the voltage on the dc bus is Vdc.

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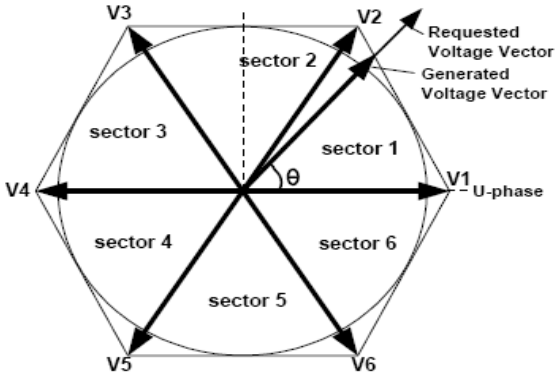
The maximum modulation, Umag L, in the linear operating range is determined by:

$$U_{mag_L} = 2^{25}*\sqrt{3}/Mod\_Scl \quad (23)$$

When Umag exceeds Lmag, we speak about over modulation. The voltage vector has now passed through the hexagonal gap in the barrier. For instance, the S VPWM algorithm will scale down the voltage vector if it's too large. The phase angle is always maintained, even if the magnitude of the voltage vector outside the hexagon. Figure 6 (SVPWM rescaling) shows what happens to the transfer gain of the PWM modulator when it is over-modulated.



Voltage rescaling (Figure 13)

After being given a modulation index, the Space Vector PWM Tm sub-module will begin calculations on the rising edge of the PWM Load signal (UAlpha and UBeta). Using a sector determination strategy, the SVPWM Tm module decides which of the six possible vectors in the active space (V1 through V6) will be used and for how long (within the context of a single PWM cycle). The zero vectors that have been stolen are also picked. When working normally, the SVPWM Tm module requires 11 clock cycles, but during extreme over modulation, it requires 35 clock cycles. As nSYNC approaches the end of the nSYNC curve, the timings and vectors available for PWM production may change. After the falling edge of the nSYNC signal, further modulation instructions cannot be carried out for at least 35 clock cycles. The above PWM waveforms are voltage vectors with their magnitudes rescaled to match a sector I position in the Space Vector plane.

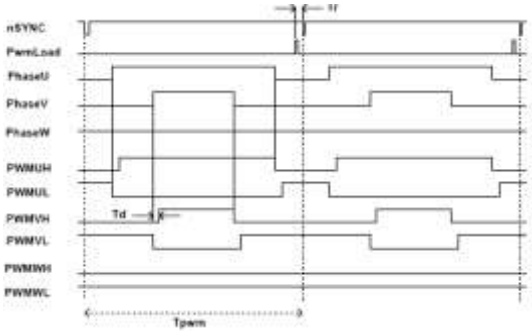


Figure 14: A Pulse Width Modulation Signal with Two Space Vectors

V. PI CONTROL USED IN MODIFIED SVPWM

We demonstrate the use of a variation of SVPWM based on PI [18, 19]. The PI control block diagram is shown in Figure 15. In S domain, the block diagram looks like this:

$$u(s) = \left[K_p + \frac{K_i}{s}\right] e(s). \quad 3$$

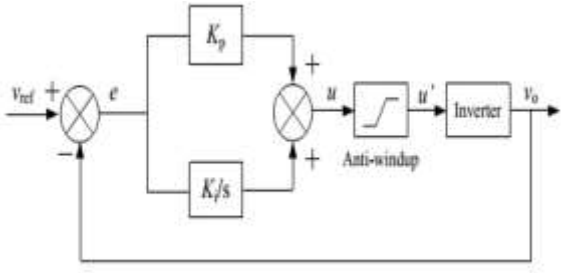
from (11), the equation can be transformed in Z domain as:

$$u(z) = \left[K_p + \frac{K_i}{1 - z^{-1}}\right] e(z) \quad 4$$

then transform (12) become difference equation is express as

$$u[n] = K_p e[n] + K_i e[n] - K_p e[n-1] + u[n-1] \quad 5$$

The control and configuration block of the system is shown in Figure 16. The system compares the voltage at the output to an established standard. Then, the system alerts the PI controller of the problem. The PI controller then communicates with the gate driver to provide a command.



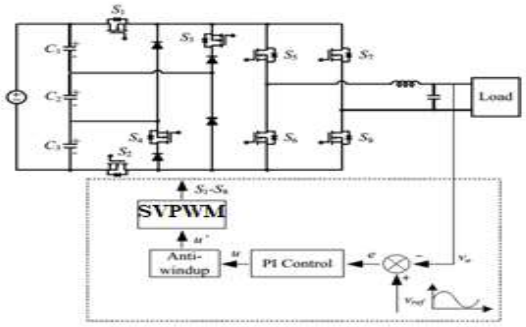


Figure 15 is a diagram of a PI control block.

In Fig. 16 we see the SVPWM control strategy applied to a seven-level inverter.

The key concept behind SVPWM is to remember the output voltage error from the previous cycle and correct it in the current cycle. To generate a sine wave at 60 hertz from a carrier frequency of 18 kHz, you'll need 300 switches.

VI Simulation Results,

The seven-level inverter's equivalent Simulink model may be seen in Figure 17. The prototype consists of a digital signal processor, gate driver, detect, and RSCC inverter with seven levels of operation.

TABLE IV

THE DESIGN DETAILS FOR THE INVERTER THAT WILL BE USED

Input voltage V_{dc}	400 V
Output voltage V_o	220 V_{rms}
Rated output power P_o	2 kW
Switching frequency f_s	18 kHz

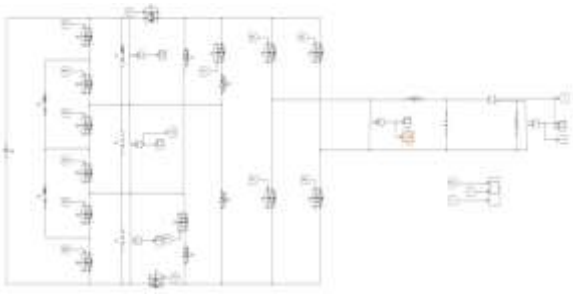


Fig. 17. MATLAB/SIMULINK circuit diagram of the proposed system

Figure 18 depicts the v ab waveform, together with the output voltage and current. Seven different voltage levels are required. Total harmonic distortion (THD) of the output voltage over all seven levels is seen in Figures 19 and 20.

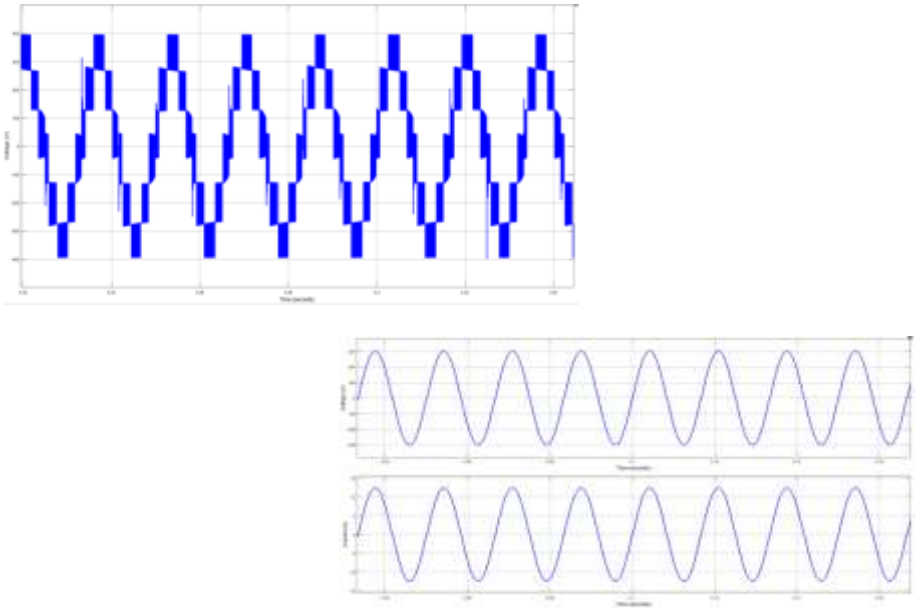


Fig. 18. Waveforms of vab, vo, and ioat

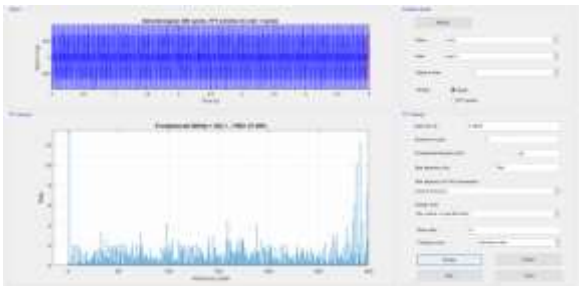


Fig. 19. FFT harmonic spectrum analysis of vat output voltage.

Figure 20: Harmonic spectrum of the output voltage

VII. CONCLUSION

In this research, a state-of-the-art seven-stage inverter is built using digital signal processing. The proposed layout attempts to reduce the total amount of power sources needed. Compared to the previous design, the new one is obviously far more energy efficient. Using a root-mean-square (rms) voltage of 220 volts, a 2-kilowatt (kW) inverter prototype has been constructed. There is a maximum input voltage of 400 V. Our analysis of the test data shows that the efficiency at full load is 94.6% and that at its peak it reaches 96.9%.

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